Assembly and Operating Instructions
CPU 8/9 SS-50 Processor Board

The CPU 8/9 SS-50 bus processor card is designed so that either a 6809, 6808, or 6802 MPU chip may be installed. The 6808 and 6802 MPUs are software compatible with the 6800 at the op-code level. This allows the CPU 8/9 to run standard 6800 software when a 6808 or 6802 MPU chip is installed. The CPU 8/9 is designed to support most standard 6809 and 6800 operating systems and monitors. A 6840 timer is included to support functions such as printer spooling and multiuser time slicing. A 1K byte RAM is also provided on board to provide a scratch area for use by system monitor ROMs. An optional baud rate generator circuit is also provided for use with systems that don't provide a baud rate generator on the mother board. The CPU 8/9 does not provide a DAT for extended addressing and therefore can't support programs that use extended addressing. The RAM and other devices on the CPU 8/9 board are private to the CPU 8/9 and can't be accessed by external DMA devices.

The CPU 8/9 provides the following features:

* The CPU 8/9 may use either the advanced 6809 processor or the 6800 compatible 6808 and 6802 processors.

* The CPU 8/9 will support most standard 6809 and 6800 software.

* A 6840 Timer chip is provided on the CPU 8/9 board.

* 1K bytes of RAM is provided on the CPU 8/9 board.

* Three sockets for 6K bytes of 2716 EPROM are provided.

* A baud rate generator is optional on the CPU 8/9.

* HALT mode DMA is supported with all processors.

* BUSREQ mode DMA is supported with the 6809 processor.

* The CPU 8/9 memory map may be changed from the standard 6809 SS-50 configuration to the traditional 6800 memory map.

Card Assembly

Before assembly of the CPU 8/9 processor card is started decisions must be made on several optional features of the CPU 8/9 card. If the a baud rate generator is not required, the parts associated with it may be omitted. These parts are indicated in the parts list. Several of the option jumpers have been preprogrammed by foil traces on the solder side of the board. These option jumpers are the ones that control the baud rate generator and allow the use of the old SS-50 UD1 and UD2 lines by the user. Consult the section describing these jumpers and determine if you will need to change the programming that is provided by the foil traces. The preprogrammed foil traces should be cut before construction starts if required.

Before construction is started both sides of the bare PC board should be carefully inspected for open traces or shorts between traces. In the the event any open traces are found they should be bridged with a fine piece of wire and solder. If any shorts are found they should be carefully scraped away with a small knife.
After the board has been inspected the following order of assembly is recommended. Carefully observe the correct orientation of sockets, diodes and the tantalum capacitors as they are installed. The sockets should be installed with their orientation mark near the pin 1 legend on the board. All sockets and other components should be inserted from the side marked "COMPONENT SIDE". All soldering should be done on the solder side of the board.

1. The CPU 8/9 uses two overlapping 40 pin socket positions for the MPU chips to prevent two MPU's from being installed at one time. Four 20 pin end stackable sockets are used to form these special overlapping 40 pin sockets. Insert and solder four 20 pin sockets in two columns between the U19 and U20 legends. If you will only be using one type of CPU you may substitute a standard 40 pin socket at U19 for the 6809 or at U20 for the 6808 or 6802 MPU.

2. Insert and solder a 28 pin socket at position U18.

3. Insert and solder 24 pin sockets at locations U10, U23, U24, and U25. The socket at U10 may be omitted if the baud rate generator is not required.

4. Insert and solder 20 pin sockets at locations U2, U3, U4, U6, U8, and U9.

5. Insert and solder 18 pin sockets at locations U21 and U22.

6. Insert and solder a 16 pin socket at location U7.

7. Insert and solder 14 pin sockets at locations U1, U5, U11, U12, U13, U14, U15, U16, and U17.

8. Insert and solder the five 10-pin Molex connectors along the bottom edge of the board. Insert the key at the position marked with a triangle on the solder side of the board.

9. Insert and solder in place header strips at locations J3, J6, J7, J8, J9, J10, J12, J13, and J14. Header strips may also be installed if required at locations J1, J2, J4, J5, and J11. If header strips are installed at these locations make sure the foil jumpers on the solder side of the board are cut first.

10. Following the values in the parts list insert and solder resistors at the locations marked on the board legend. R10 and R16 may be deleted if the baud rate generator option is not installed.

11. Insert and solder diode D1 at the location marked on the board legend. Note that the diode should be oriented so the arrow on legend points toward the banded end of the diode.

12. Following the values in the parts list insert and solder tantalum capacitors C28, C29, and C30 at the locations indicated on the board legend. Note that the tantalum capacitors must be oriented so their positive end is aligned with the "+" on the board legend.

13. Insert and solder mica capacitors C26 and C27.

14. Insert and solder bypass capacitors C1 through C25. Bypass capacitors C1 and C10 may be omitted if the optional baud rate generator is not required.

15. Insert and solder XTL2 being careful that the case of XTL2 does not short to any of the foils on the top of the board.

16. Bend the leads of XTL1 perpendicular to the case; insert the leads through the board at the position marked on the board legend. The body of XTL1 should be flat against the board. Strap XTL1 to the board by means of a piece of wire inserted in the holes on each side of XTL1 and pulled tight against the body. Solder the two leads of XTL1 and the two ends of the wire strapping it down. XTL1 may be deleted if the baud rate generator is not required.

17. Mount the Heatsink to the component side of the board with four 6-32 x 5/16 inch screws, using lock washers and nuts on the solder side of the board.

18. Mount the voltage regulator to the heatsink using 6-32 x 3/8 inch screws and hardware. A heat conductive compound should be used between the heatsink and regulator. The two leads of the regulator should pass through the board and be soldered on the solder side of the board.

19. At this time the board is complete with the exception of inserting the ICs and the jumper shunts. The voltage regulator should now be tested by pluging the CPU 8/9 board into a SS-50 mother board. Turn the power supply on and measure the voltage at pin 18 of U21. This voltage should be between 4.75 volts and 5.25 volts. If it is not correct the regulator may be bad and should be replaced. If the voltage is near zero it is possible that there is a shorted 5 volt line on the board. Correct any problem before proceeding.

20. Following the parts list insert ICs U1 through U18 and U21 through U22 in their sockets. Make sure pin 1 of each IC is adjacent to the pin 1 mark on the board legend. ICs U1 and U10 may be omitted if the baud rate generator on the CPU 8/9 is not required.

21. If you will be using a 6809 MPU it should now be installed at location U19. If are using a 6808 or 6802 install it at location U20. In either case take care that pin 1 is correctly aligned.

22. Install your monitor ROM or EPROM at location U23.

23. After reading the description of the option jumpers on pages 6 through 9 configure the jumpers as required for your system. Some typical settings for 6809 and 6808 systems are given in the table on page 5. These should work for most systems.

24. Removing U1 will eliminate the CPU generated baud rate signals from the bus if necessary.

25. Congratulations! Your CPU 8/9 is now complete and ready for installation in your system.

Monitor ROMs and DOS

The CPU 8/9 can be used with most 6809 and 6800 monitor ROMs. Check with your dealer for a monitor suitable for your needs. When the CPU 8/9 is operating in the 6800 compatible 6808 mode the monitor ROM at U23 is decoded so it will respond to addresses E000 - E7FF as well as to its normal addresses F800 - FFFF. This permits the use of traditional 6800 monitor programs.

Monitor ROMs designed for systems with a DAT will usually work without any problem unless you plan on running a DOS that uses a DMA type disk controller. If you will be using a DMA disk controller on a 6809 system make sure that the LOGICAL to REAL ADDRESS conversion subroutine (LRA) in your monitor ROM is designed to operate properly in a system without a DAT. Most work correctly but a few don't.

Many of the popular disk operating systems for the 6800 require that memory be installed at addresses A000 - BFFF for use by the DOS. If this is the case the 1K RAM on the CPU 8/9 board must be disabled by removing jumper connecting jumper J10-11 to J10-12. This is because the RAM on the CPU card is incompletly decoded in 6808 mode and it interferes with the off board memory in the range of A400 - A7FF.

CPU 8/9 MEMORY MAP

Device	6809 mode Address	6808 mode Address
EPROM at U23	F800 - FFFF	F800 - FFFF and E000 - E7FF
EPROM at U24	F000 - F7FF	F000 - F7FF
EPROM at U25	E800 - EFFF	E800 - EFFF
1K byte RAM	E400 - E7FF	A000 - A3FF alias A400 - A7FF
6840 TIMER	E210 - E217	82B0 - 82B7

TYPICAL JUMPER SETTINGS

This table gives the recommended jumper settings for several CPU chip and bus combinations. Details are on the following pages.

CPU 8/9 Jumper	6809 SS50-C	6808 SS50-C	6808 SS50	Notes
J1	2 to 3	2 to 3	1 to 2	Note 1
J2	2 to 3	2 to 3	1 to 2	Note 1
J3	1 to 2	1 to 2	2 to 3	
J4	1 to 2	1 to 2	none	Note 2
J5	1 to 2	1 to 2	none	Note 2
J6	2 to 3	2 to 3	2 to 3	
J7	2 to 3	2 to 3	1 to 2	
J8	1 to 2	1 to 3	1 to 3	
J8	3 to 4	2 to 4	2 to 4	
J8	5 to 6	5 to 7	5 to 7	
J8	7 to 8	6 to 8	6 to 8	
J8	9 to 10	9 to 10	9 to 10	
J9	1 to 2	none	none	
J10	3 to 4	1 to 2	1 to 2	
J10	5 to 6	5 to 6	5 to 6	
J10	7 to 8	7 to 8	7 to 8	
J10	9 to 10	11 to 12	11 to 12	Note 3
J10	13 to 14	13 to 14	13 to 14	Note 4
J11	1 to 2	1 to 2	1 to 2	Note 1
J12	1 to 3	1 to 3	3 to 5	
J13	Front Panel Conn.		none	
J14	MC6840 Timer I/O Connector			

Note 1: These jumpers control the optional baud rate generator. They are preprogrammed by foil traces for the standard SS50-C baud rates. The foil traces must be cut if the baud rates are to be changed.

Note 2: These jumpers may be removed to disable the SS50-C FIRQ and Q signals from the bus. They are preprogrammed by foil traces which must be cut to use the SS50 bus UD2 and UD1 lines.

Note 3: Connecting J10-9 to J10-10 enables the 1K on board RAM at E400 - E7FF for use with the 6809. Connecting J10-11 to J10 - 12 enables the RAM at A000-A7FF for use with 6808 systems. Do not install a jumper at either of these positions if these addresses are incompletely decoded by the mother board or are used elsewhere in the system. Also note that the RAM is incompletely decoded in 6808 mode.

Note 4: Connecting a jumper from J10-13 to J10-14 enables the 6840 timer chip at the address selected by jumper area J8. The standard address is E210 for 6809 systems and 82B0 for 6808 systems. Do not install this jumper if these addresses are used eleswhere in the system or are incompletely decoded by the mother board.

JUMPER OPTIONS

The CPU 8/9 has a number of option jumpers which must be correctly set before the CPU can be used. Typical settings for these jumpers are given on the preceding page. These settings will provide a workable starting point for many systems. If you have any special system requirements the following section contains the information you will require for selecting the proper jumper options.

4800/600 Baud Option Jumper (J1)

This option selects either 4800 baud or 600 baud output on the bus 4800/600 baud line. You must have the optional baud rate generator installed on your CPU 8/9 board for this jumper to function. This option jumper is preprogrammed for 4800 baud by a foil trace on the solder side of the board. This foil trace between J1-2 and J1-3 must be cut if the 600 baud option is to be selected.

Connect J1-2 to J1-3 for 4800 baud.
Connect J1-1 to J1-2 for 600 baud.

9600/150 Baud Option Jumper (J2)

This option selects either 9600 baud or 150 baud output on the bus 9600/150 baud line. You must have the optional baud rate generator installed on your CPU 8/9 board for this jumper to function. This option jumper is preprogrammed for 9600 baud by a foil trace on the solder side of the board. This foil trace between J2-2 and J2-3 must be cut if the 150 baud option is to be selected.

Connect J2-2 to J2-3 for 9600 baud.
Connect J2-1 to J2-2 for 150 baud.

BUSREQ/110 Option Jumper (J3)

This option jumper allows the BUSREQ/110 bus line to be used as the BUSREQ input for 6809 DMA, or as a 110 baud output from the optional baud rate generator.

Connect J3-1 to J3-2 for use as 6809 BUSREQ.
Connect J3-2 to J3-3 for 110 baud output.

Q/UD1 Option Jumper (J4)

This option jumper connects the 6809 Q signal to the bus. This jumper may be removed to convert this bus line for use as the UD1 line. This line is preprogrammed to be the Q output by a foil trace on the solder side of the board. This foil trace between J4-1 and J4-2 must be cut if this bus line is to be used as the UD1 line.

Connect J4-1 to J4-2 for 6809 Q output.
Remove J4-1 to J4-2 jumper for use as UD1.

FIRQ/UD2 Option Jumper (J5)

This option jumper connects the 6809 FIRQ signal to the bus. This jumper may be removed to convert this bus line for use as the UD2 line. This line is preprogrammed to be the FIRQ input by a foil trace on the solder side of the board. This foil trace between J5-1 and J5-2 must be cut if this bus line is to be used as the UD2 line.

Connect J5-1 to J5-2 for 6809 FIRQ input.
Remove J5-1 to J5-2 jumper for use as UD2.

IRQ/FIRQ Timer Interupt (J6)

The 6840 timer interrupt request line may be connected to either the processor IRQ or to the FIRQ by means of this option jumper. When using a 6808 or 6802 processor the IRQ option should be selected as these processors don't have FIRQ inputs.

Connect J6-1 to J6-2 for Timer FIRQ.
Connect J6-2 to J6-3 for Timer IRQ.

MRDY/MRST Option Jumper (J7)

Many peripheral cards such as disk controllers do not operate properly at clock rates above 1 MHz. The MRDY line is provided to stretch the processor clock when these devices are accessed. This option works with both the 6809 processor and the 6800 compatible 6808 processor.

Older SS-50 bus computers connect the front panel RESET button to this bus line. The MRST Option allows use of this bus line in these older computers as the front panel RESET button input line.

Connect J7-2 to J7-3 for use as Memory Ready.
Connect J7-1 to J7-2 for use as Front Panel RESET button input.

TIMER ADDRESS Option Jumpers (J8)

The Programmable Timer may be placed at several different addresses by means of this jumper area. The following table shows the required jumpers for each of the 10 addresses that can be selected by this jumper area. The most useful address for 6809 systems is E210. For 6808 systems address 82B0 is the most useful.

E210	Connect	1	to	2,	3	to	4,	5	to	6, 7 to 8, and 9 to 10.
E090	Connect	1	to	2,	3	to	9,	4	to	10, 5 to 6, and 7 to 8.
E030	Connect	1	to	2,	3	to	4,	5	to	6, 7 to 9, and 8 to 10.
C290	Connect	1	to	2,	3	to	5,	4	to	6, 7 to 8, and 9 to 10.
C230	Connect	1	to	2,	3	to	4,	5	to	7, 6 to 8, and 9 to 10.
C0B0	Connect	1	to	2,	3	to	5,	4	to	6, 7 to 9, and 8 to 10.
A290	Connect	1	to	3,	2	to	4,	5	to	6, 7 to 8, and 9 to 10.
A230	Connect	1	to	10,	2	to	4,	3	to	8, 5 to 6, and 7 to 9.
A0B0	Connect	1	to	3,	2	to	4,	5	to	6, 7 to 9, and 8 to 10.
82B0	Connect	1	to	3,	2	to	4,	5	to	7, 6 to 8, and 9 to 10.

6808/6809 DMA Option Jumper (J9)

The 6808 and 6809 processors have different DMA handshake timing requirements. This jumper option adjusts the DMA circuits on the CPU 8/9 to meet these requirements.

Connect J9-1 to J9-2 for 6809 DMA Timing.
Remove J9-1 to J9-2 for 6808 (6802) DMA Timing.

DEVICE ENABLE Option Jumpers (J10)

The option jumpers in this area provide the ability to enable or disable the devices on the CPU 8/9 board. These devices include the three 2716 EPROM sockets, the 1K byte RAM, and the 6840 timer chip. Two option jumpers are provided for the EPROM at location U23. This EPROM may be enabled to respond at address locations F800 - FFFF or to respond at F800 - FFFF and E000 - E7FF for use with 6800 type monitor programs. The 1K RAM may be selected at addresses E400 -E7FF for 6809 systems or at A000 - A3FF for 6800 systems. Due to incomplete address decoding, the RAM will also respond at addresses A400 - A7FF when set to respond at A000 - A3FF. Both the EPROM at U23 and the 1K RAM should have only one of their 2 jumper options installed at a time.

Connect J10-1 to J10-2 Enable EPROM U23 at F800-FFFF & E000-E7FF.
Connect J10-3 to J10-4 Enable EPROM U23 at F800-FFFF only.
Connect J10-5 to J10-6 Enable EPROM U24 at F000-F7FF.
Connect J10-7 to J10-8 Enable EPROM U25 at E800-EFFF.
Connect J10-9 to J10-10 Enable 1K RAM at E400-E7FF only.
Connect J10-11 to J10-12 Enable 1K RAM at A000-A3FF & A400-A7FF.
Connect J10-13 to J10-14 Enable Timer at address selected by (J8).

HI/LO BAUD Option Jumper (J11)

The optional baud rate generator on the CPU 8/9 board may be operated at 4 times the normal rate by removing this jumper. This jumper is preprogrammed for normal operation by foil trace on the solder side of the board. This foil trace must be cut to operate at the HI baud rates.

Connect J11-1 to J11-2 Enable LO baud rates.
Remove J11-1 to J11-2 Enable HI baud rates.

NMI SOURCE Option Jumper (J12)

The source for NMI interrupts to the CPU 8/9 may come from one of three places. The first source is the front panel NMI/ABORT button. The second NMI source is the NMI bus line defined on the original SS-50 bus. The final NMI source is the #1 Timer output. Some monitor programs use this timer NMI to provide a single step or trace function. Only one NMI option jumper may be connected.

Connect J12-1 to J12-3 NMI source is front panel button.
Connect J12-3 to J12-5 NMI source is bus BUSY/NMI.
Connect J12-4 to J12-6 NMI source is #1 timer output.

FRONT PANEL and TIMER CONNECTORS

FRONT PANEL CONNECTOR (J13)

The connector from a front panel RESET and NMI/ABORT button may be connected to this header area. An alignment key is provided to insure the proper orientation of the front panel connector.

J13-1	Front panel RESET input
J13-2	KEY
J13-3	Front panel RESET ground
J13-4	Front panel NMI/ABORT ground
J13-5	Front panel NMI/ABORT input

TIMER CONNECTOR (J14)

This connector provides access to the 6840 timer I/O lines. All three timer outputs from the 6840 are available on this connector. The external clock and gate inputs for timers #2 and #3 are also available on this connector. The gate inputs must be at ground level for timers #2 and #3 to operate. The gate inputs may be grounded by means of jumper shunts if a connector to an external device is not used. The external clock and gate inputs for timer #1 are grounded on the board and are not available at the connector.

J14-1	Not Used
J14-2	Ground
J14-3	Timer #3 output
J14-4	Ground
J14-5	Timer #3 Gate input
J14-6	Ground
J14-7	Timer #3 External Clock input
J14-8	Ground
J14-9	Timer #2 output
J14-10	Ground
J14-11	Timer #2 Gate input
J14-12	Ground
J14-13	Timer #2 External Clock input
J14-14	Ground
J14-15	Timer #1 output
J14-16	Ground
J14-17	Not Used
J14-18	Ground
J14-19	Not Used
J14-20	Ground

The three timers in the 6840 may be cascaded by making the following jumper connections.

Connect J14-5 to J14-6.
Connect J14-7 to J14-9.
Connect J14-11 to J14-12.
Connect J14-13 to J14-15.

SS-50 BUS PIN ASSIGNMENTS

Pin	Mnemonic	Signal Description
1	D0	Data Bus Bit 0
2	D1	Data Bus Bit 1
3	D2	Data Bus Bit 2
4	D3	Data Bus Bit 3
5	D4	Data Bus Bit 4
6	D5	Data Bus Bit 5
7	D6	Data Bus Bit 6
8	D7	Data Bus Bit 7
9	A15	Address Bus Bit 15
10	A14	Address Bus Bit 14
11	A13	Address Bus Bit 13
12	A12	Address Bus Bit 12
13	A11	Address Bus Bit 11
14	A10	Address Bus Bit 10
15	A9	Address Bus Bit 9
16	A8	Address Bus Bit 8
17	A7	Address Bus Bit 7
18	A6	Address Bus Bit 6
19	A5	Address Bus Bit 5
20	A4	Address Bus Bit 4
21	A3	Address Bus Bit 3
22	A2	Address Bus Bit 2
23	A1	Address Bus Bit 1
24	A0	Address Bus Bit 0
25	GND	Ground
26	GND	Ground
27	GND	Ground
28	+8 Volts	Unregulated 8 Volt supply
29	+8 Volts	Unregulated 8 Volt supply
30	+8 Volts	Unregulated 8 Volt supply
31	-16 Volts	Unregulated -16 Volt supply
32	+16 Volts	Unregulated +16 Volt supply
33	INDEX	Index Key
34	MRDY/MRST	Ready line or optional RESET input
35	BUSY/NMI	Busy line or optional NMI input
36	IRQ	Interrupt Request input
37	FIRQ/UD2	Fast Interrupt or optional User Defined line.
38	Q/UD1	Q Clock output or optional User Defined line.
39	E	E Clock output
40	VMA	Valid Address output
41	R/W	Read Write line
42	RESET	RESET output line from CPU
43	BA	Bus Available output from processor
44	BS	Bus Status output from 6809
45	HALT	HALT input to processor
46	BUSREQ/110b	Bus Request input to 6809 or 110 baud output
47	9600b/150b	9600 or 150 baud output
48	300b	300 baud output
49	4800b/600b	4800 or 600 baud output
50	1200b	1200 baud output

Parts List
CPU 8/9

Resistors

R1,R2,R3,R4,R6,R7	5.6K ohm 1/4 watt resistor
R8,R9,R16,R17,R19	5.6K ohm 1/4 watt resistor
R24,R25,R26,R27	5.6K ohm 1/4 watt resistor
R5,R11,R12,R13	3.3K ohm 1/4 watt resistor
R14,R15	3.3K ohm 1/4 watt resistor
R10	10 meg ohm 1/4 watt resistor
R18	12K ohm 1/4 watt resistor
R20,R21	100 ohm 1/4 watt resistor
R22,R23	390K ohm 1/4 watt resistor

Capacitors

C1,C2,C3,C4,C5,C6	0.047 mfd disc capacitor
C7,C8,C9,C10,C11	0.047 mfd disc capacitor
C12,C13,C14,C15,C16	0.047 mfd disc capacitor
C17,C18,C19,C20,C21	0.047 mfd disc capacitor
C22,C23,C24,C25	0.047 mfd disc capacitor
C26,C27	24 pfd mica capacitor
C28,C29	1.0 mfd 25 volt tantalum capacitor
C30	2.2 mfd 25 volt tantalum capacitor

Integrated Circuits

U1,U13	74LS04 Hex Inverter
U2,U4,U6	74LS244 Octal Buffer
U3,U8,U9	74LS240 Octal Inverting Buffer
U5	74LS260 Dual NOR gate
U7	74LS138 1 of 8 Decoder
U10	MC14411 Baud Rate Generator
U11	74LS74 Dual D Flip-Flop
U12,U15	74LS00 Quad NAND gate
U14,U16	74LS30 NAND gate
U17	MC14584 CMOS Hex Schmitt trigger
U18	MC6840 Triple Timer
U19	MC6809 Microprocessor
U20	MC6808 or 6802 Microprocessor
U21,U22	21L14 (300 ns) 1K x 4 RAM
U23,U24,U25	2716 (450 ns) EPROM (single supply)
U26	7805K +5 volt regulator

Miscellaneous

D1	1N4148 Diode
XTL1	1.8432 MHz crystal (parallel resonant)
XTL2	4.0 MHz crystal (parallel resonant)
Qty. 5	10-pin female Molex connector
Qty. 1	Molex key
Qty. 1	28-pin DIP socket
Qty. 4	24-pin DIP socket
Qty. 4	20-pin DIP socket, end stackable
Qty. 6	20-pin DIP socket
Qty. 2	18-pin DIP socket
Qty. 1	16-pin DIP socket
Qty. 9	14-pin DIP socket
Qty. 1	10x2 header strip
Qty. 1	7x2 header strip
Qty. 1	5x2 header strip
Qty. 1	3x2 header strip
Qty. 1	5x1 header strip
Qty. 3	3x1 header strip
Qty. 1	2x1 header strip
Qty. 19	programming shunt
Qty. 1	THM 6001-2 Heatsink
Qty. 4	6-32 x 5/16 screw
Qty. 2	6-32 x 3/8 screw
Qty. 6	6-32 nut
Qty. 6	#6 Internal Lock Washer

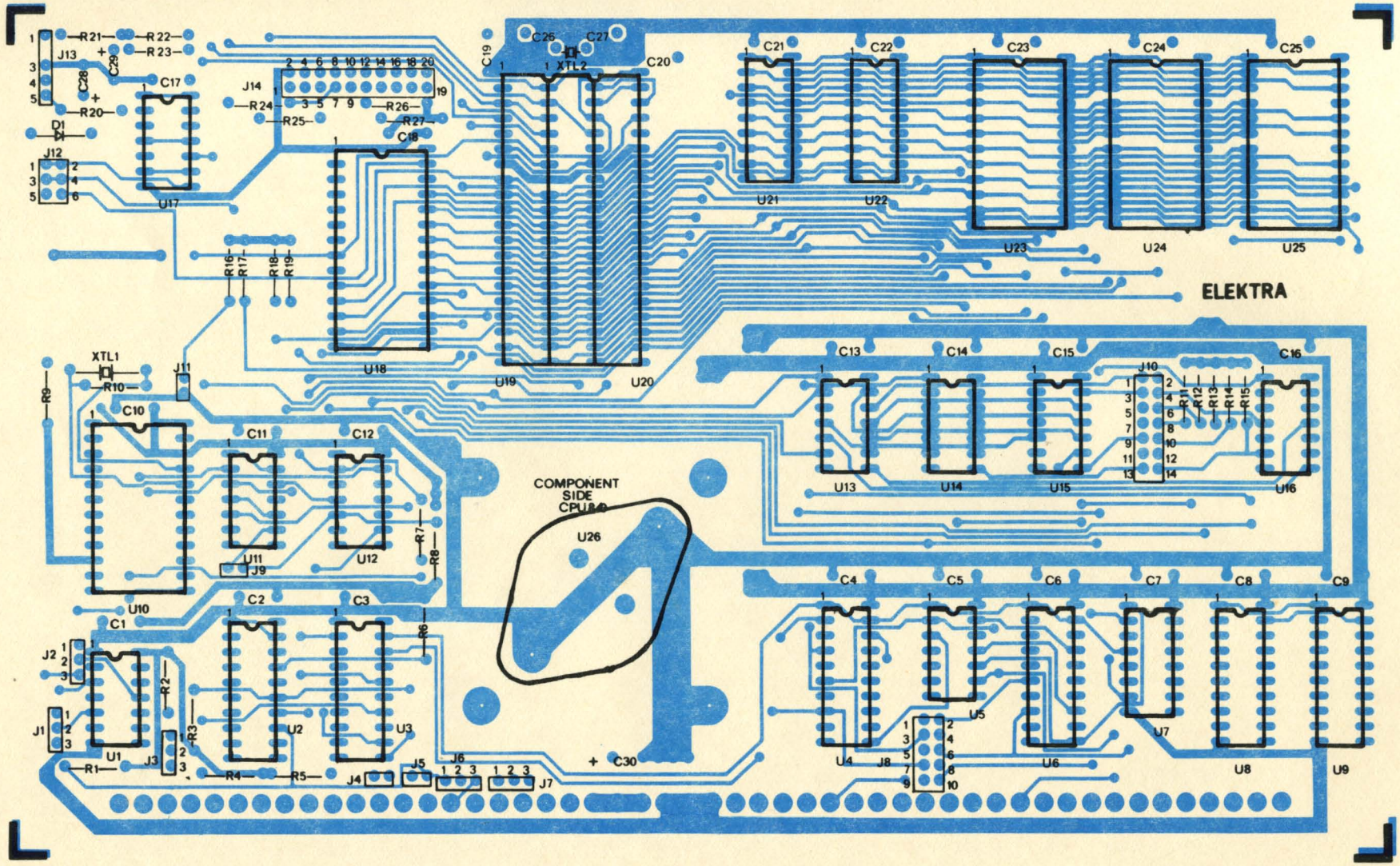
NOTE 1: The header strips come in standard lengths which can be cut to the required length.

NOTE 2: The following components may be deleted if the optional Baud Rate Generator circuit is not required.

R10,R16,C1,C10,U1,U10,XTL1

NOTE 3: Your CPU 8/9 can be converted for operation at 2 MHz by making the following component substitutions. Unfortunately at the current time, the fastest available 21L14 and 2716 memory chips are 200ns and 350ns respectively. Depending upon the performance of the chips installed, the CPU 8/9 may or may not run reliably at 2 MHz.

C26,C27	18 pfd mica capacitor
U18	MC68B40 Triple Timer
U19	MC68B09 Microprocessor
U20	MC68B08 or MC68B02 Microprocessor
U21,U22	21L14 (150 ns) 1K x 4 RAM
U23,U24,U25	2716 (250 ns) EPROM (single supply)
XTL2	8.0 MHz crystal (parallel resonant)

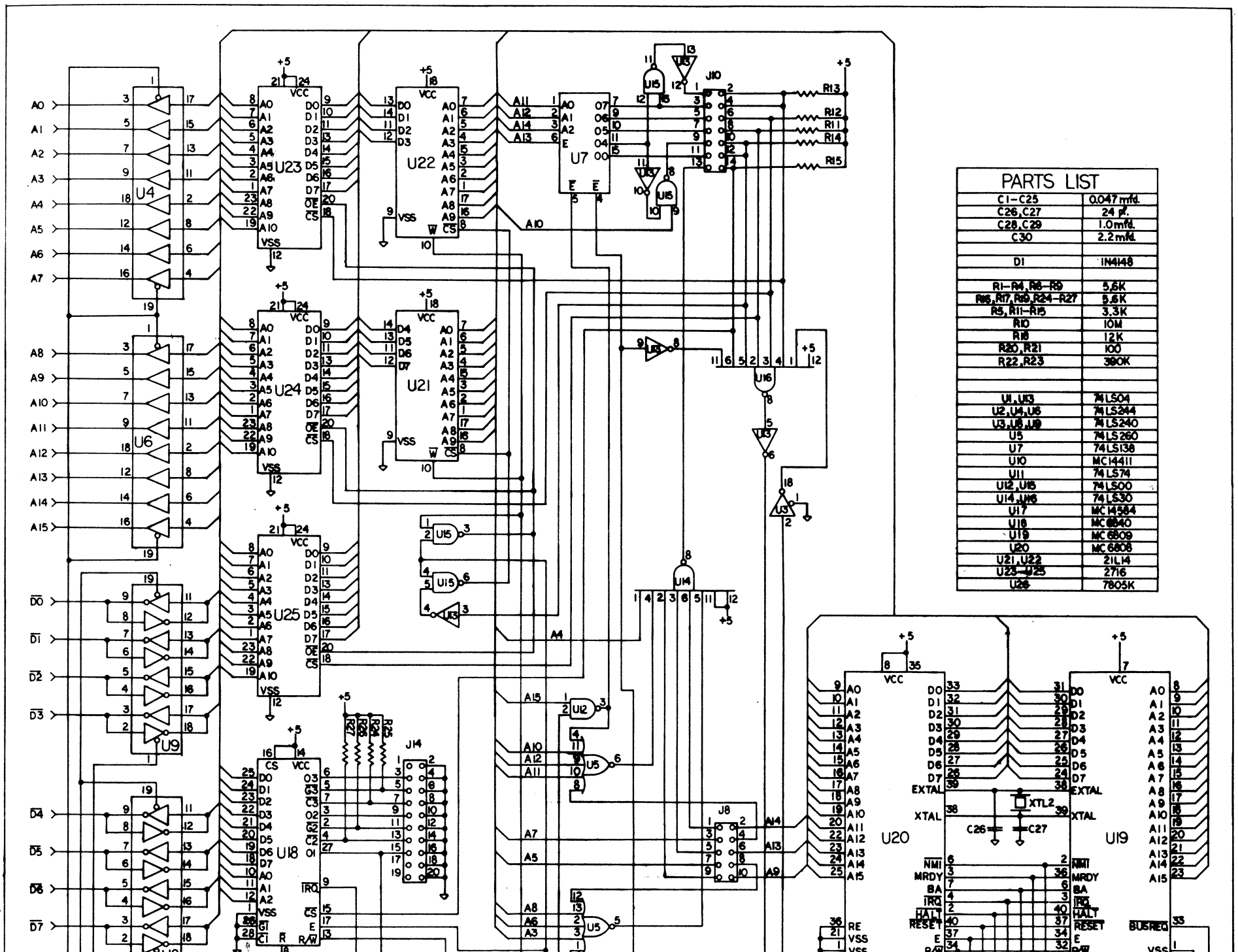


COMPONENT SIDE

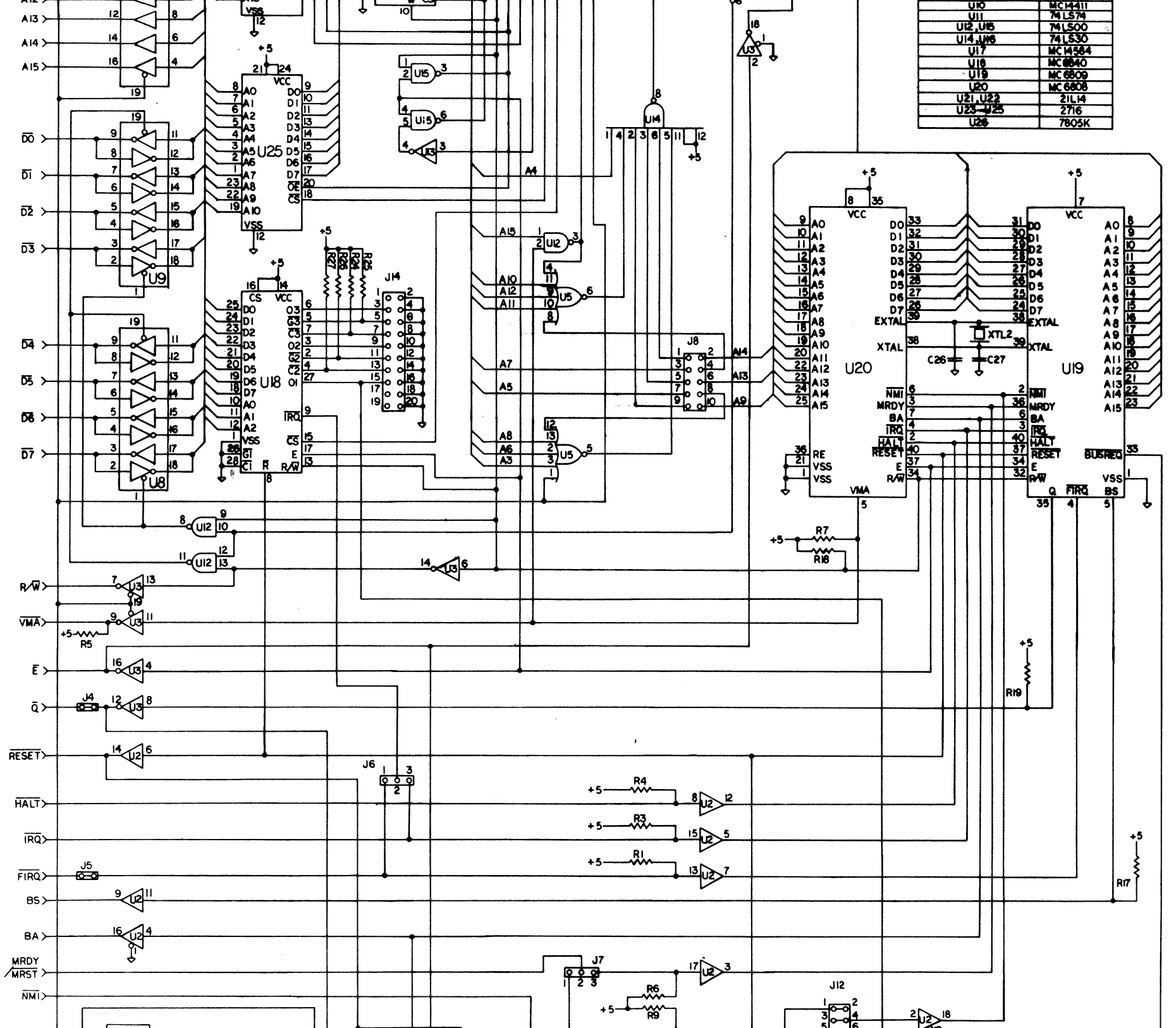
COMPONENT SIDE
SILK SCREEN

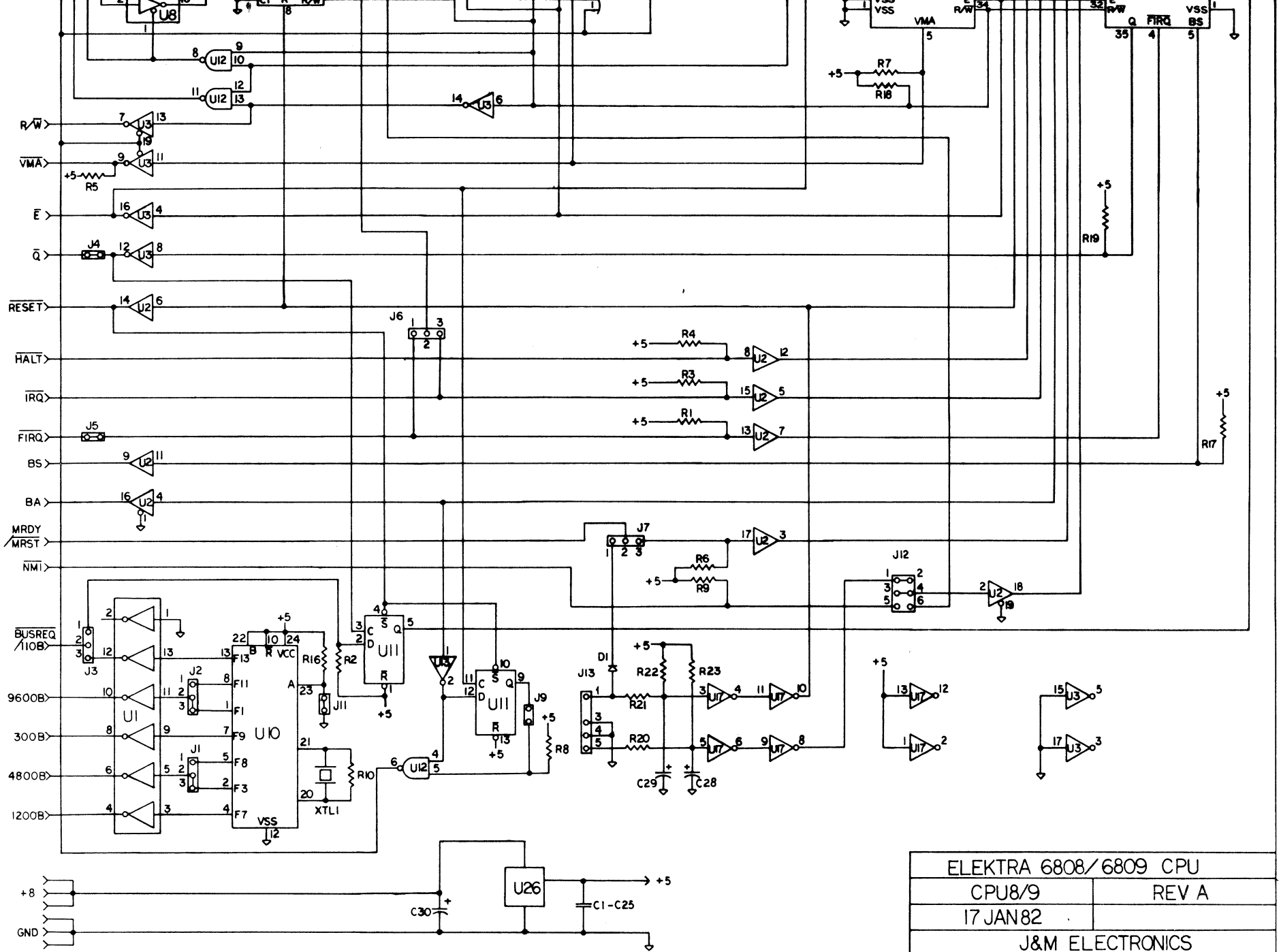
AAA CHICAGO COMPUTER CENTER
120 CHESTNUT LANE
WHEELING, IL 60090
PHONE (312) 459-0450

ELEKTRA CPU8/9
REV A | 17 JAN 82
J&M ELECTRONICS

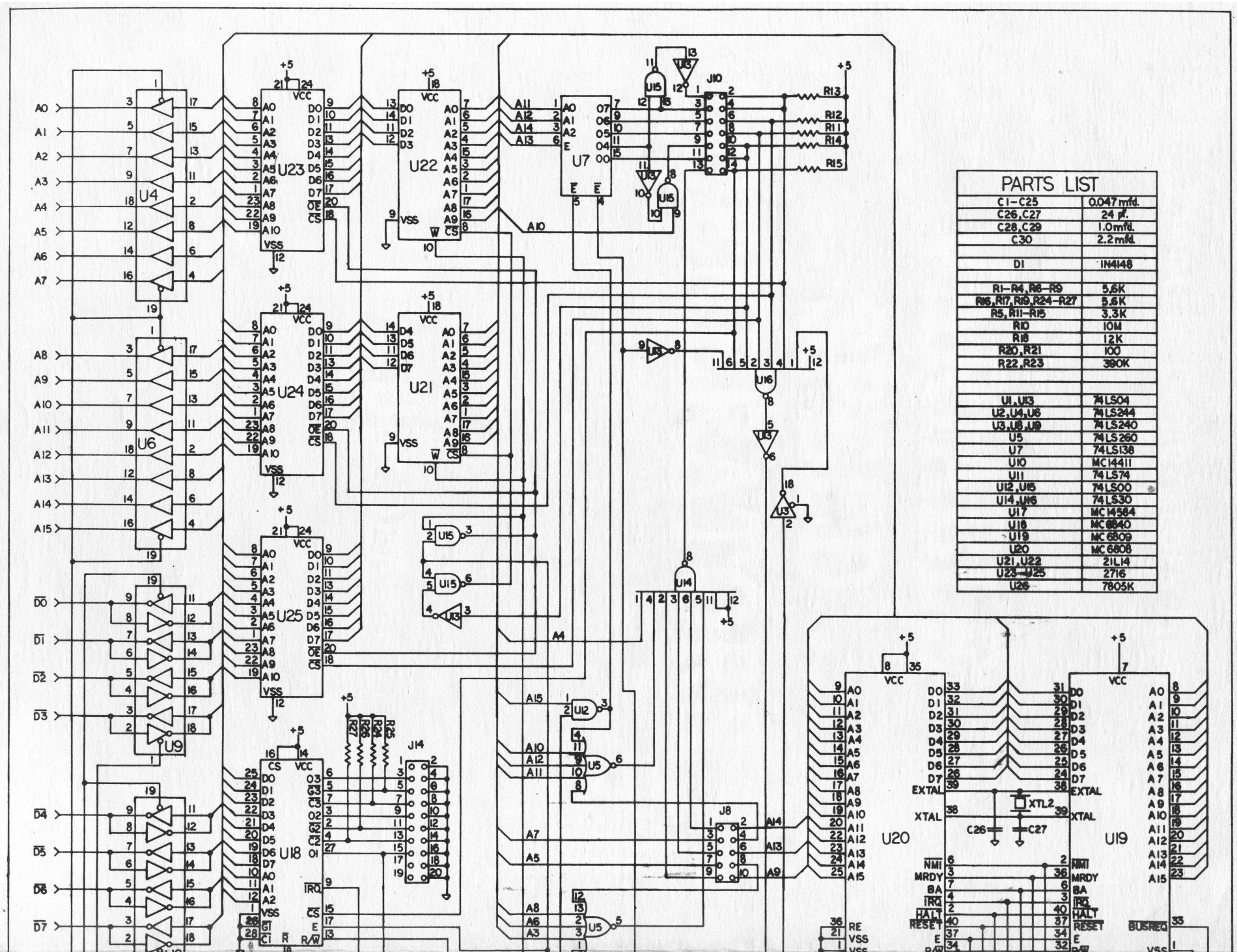


PARTS LIST	
C1-C25	0.047 mfd.
C26, C27	24 pf.
C28, C29	1.0 mfd.
C30	2.2 mfd.
D1	IN4148
R1-R4, R8-R9	5.6K
R6, R7, R9, R24-R27	5.6K
R5, R11-R15	3.3K
R10	10M
R16	12K
R20, R21	100
R22, R23	390K
U1, U3	74LS04
U2, U4, U6	74LS244
U3, U8, U9	74LS240
U5	74LS260
U7	74LS138
U10	MC14411
U11	74LS74
U12, U15	74LS00
U14, U16	74LS30
U17	MC14584
U18	MC6840
U19	MC6809
U20	MC6808
U21, U22	21L14
U23-U25	2716
U26	7805K

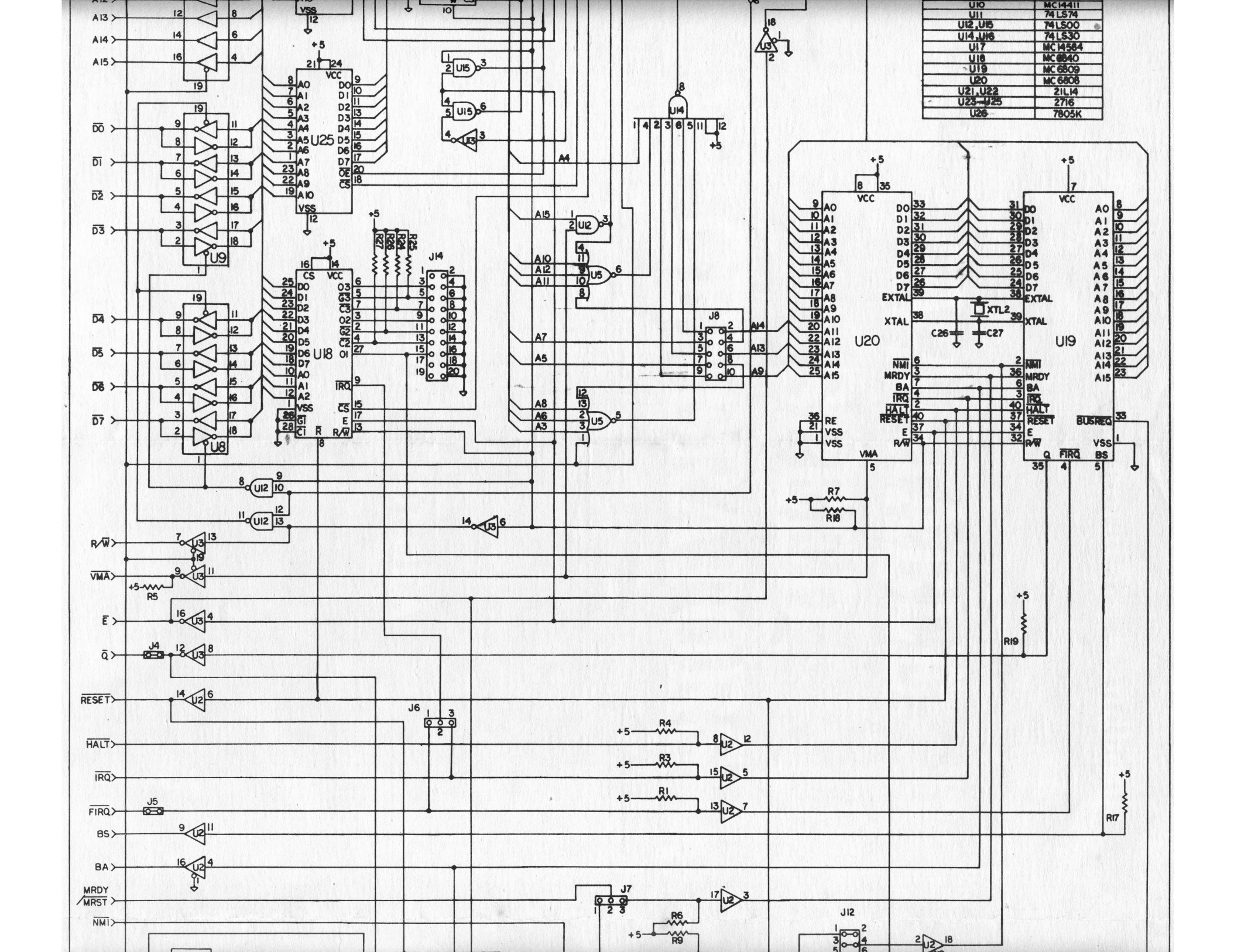

U10 MC14411
U11 74LS74
U12,U15 74LS00
U14,U16 74LS30
U17 MC14584
U18 MC6840
U19 MC6809
U20 MC6808
U21,U22 21L14
U23-U25 2716
U26 7805K
A13
A14
A15
D0
D1
D2
D3
D4
D5
D6
D7
U9
U8
U25
U18
U20
U19
J14
J8
J6
J4
J5
J7
J12
XTL2
C26
C27
R5
R7
R18
R19
R17
R4
R3
R1
R6
R9
R/W
VMA
E
Q
RESET
HALT
IRQ
FIRQ
BS
BA
MRDY
MRST
NMI
BUSREQ

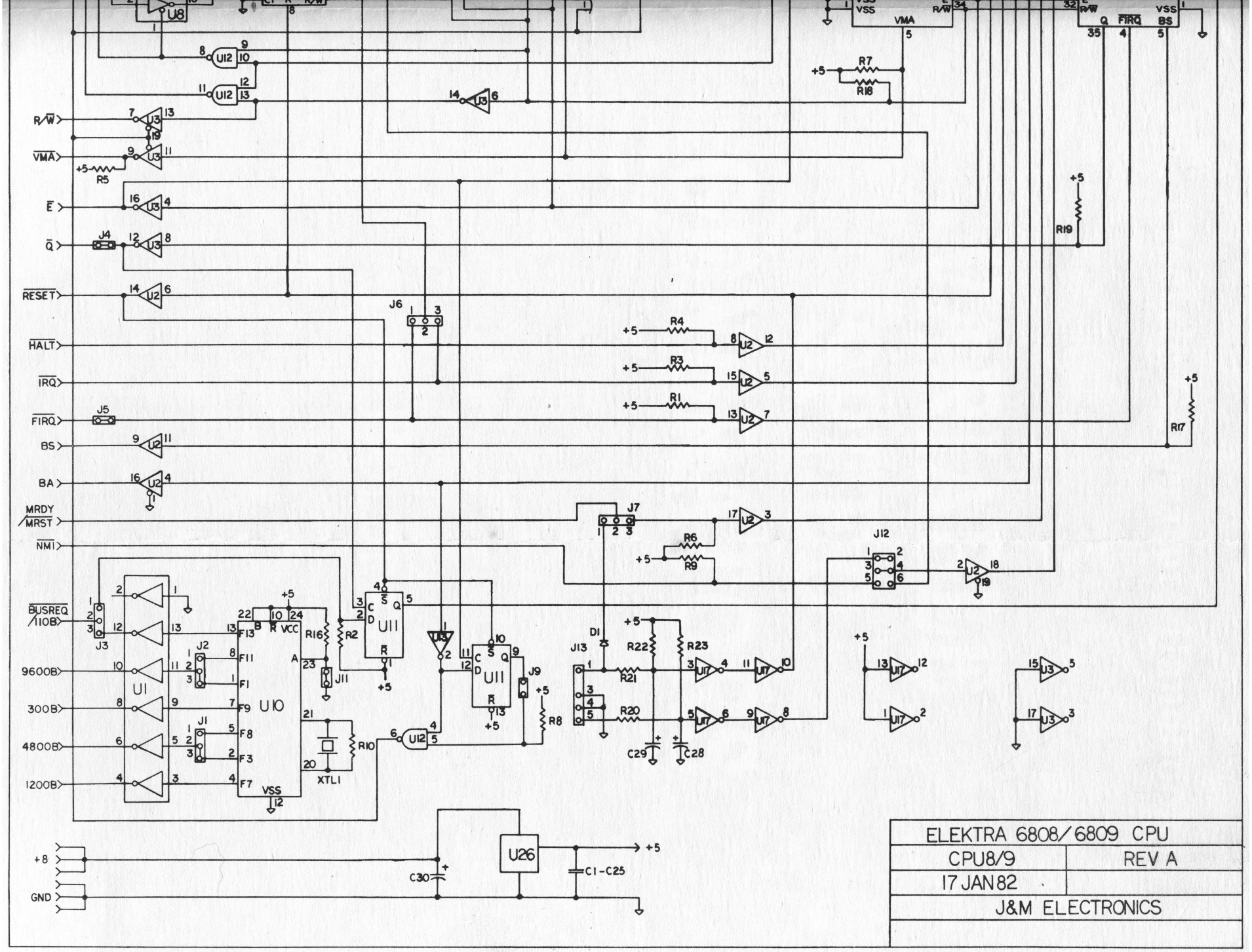


ELEKTRA 6808/6809 CPU	
CPU8/9	REV A
17 JAN 82	
J&M ELECTRONICS	

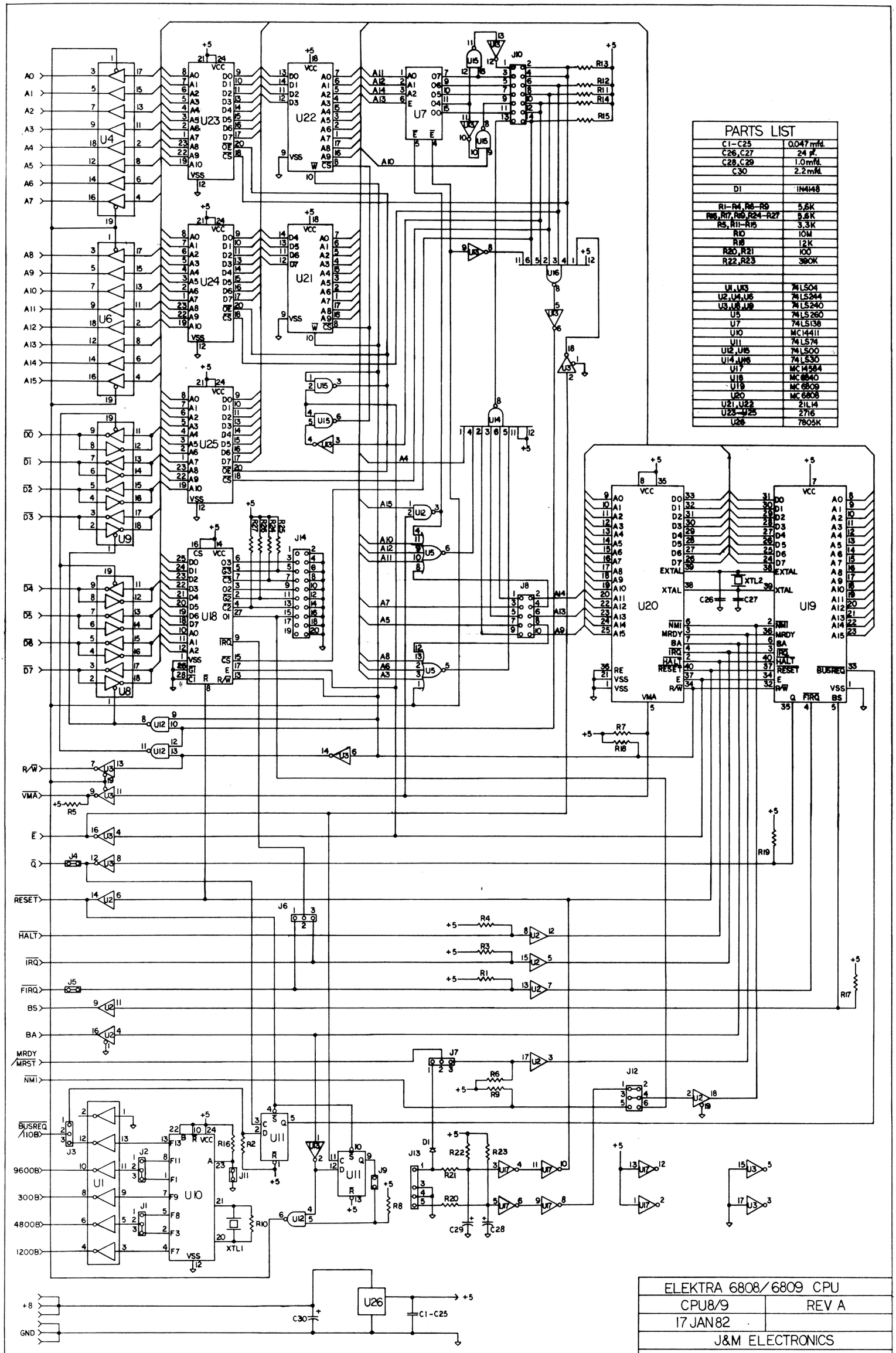


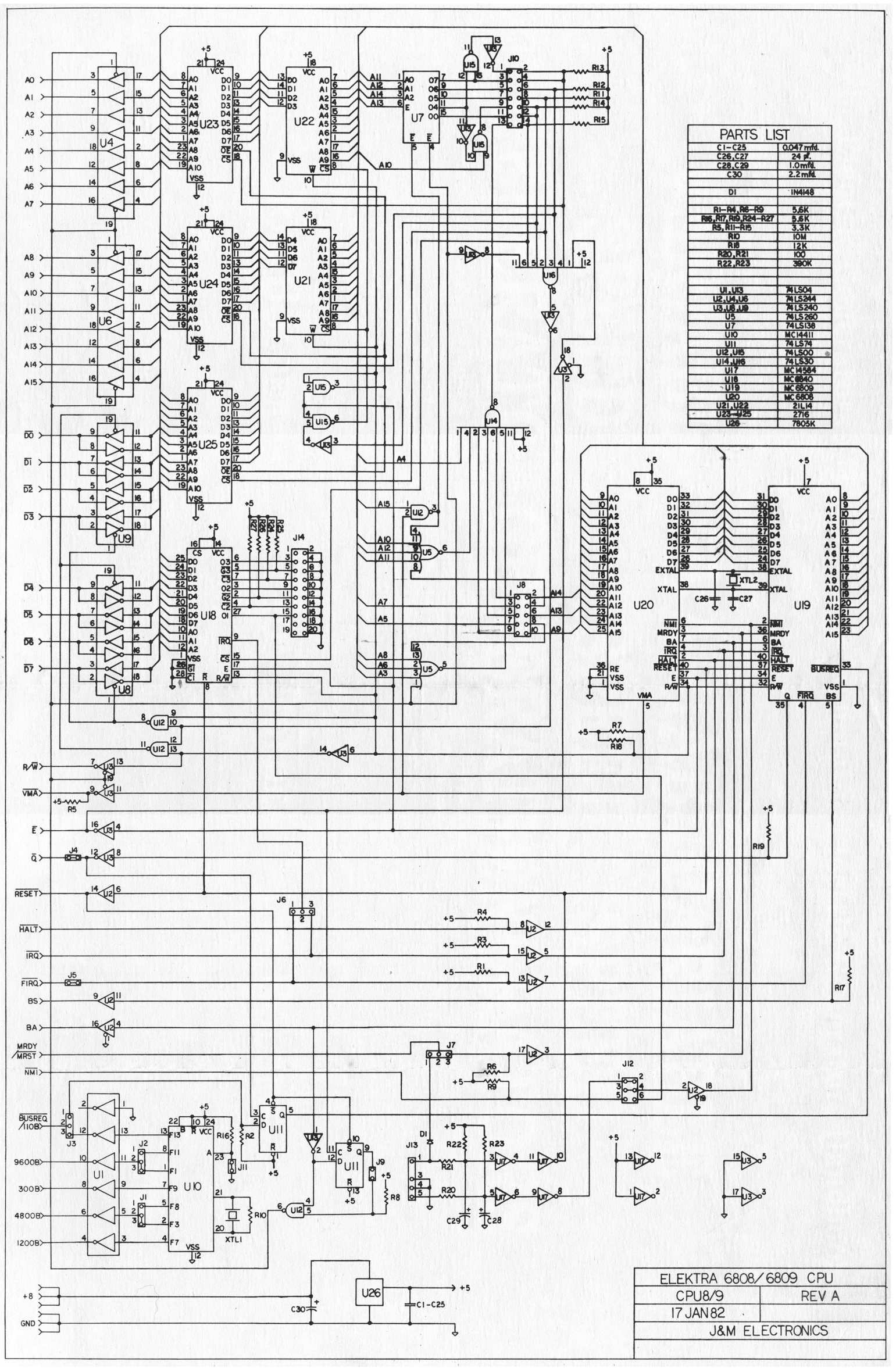
PARTS LIST	
C1-C25	0.047 mfd.
C26, C27	24 pf.
C28, C29	1.0 mfd.
C30	2.2 mfd.
D1	IN4148
R1-R4, R6-R9	5.6K
R16, R17, R19, R24-R27	5.6K
R5, R11-R15	3.3K
R10	10M
R18	12K
R20, R21	100
R22, R23	390K
U1, U13	74LS04
U2, U4, U6	74LS244
U3, U8, U9	74LS240
U5	74LS260
U7	74LS138
U10	MC14411
U11	74LS74
U12, U15	74LS00
U14, U16	74LS30
U17	MC14584
U18	MC6840
U19	MC6809
U20	MC6808
U21, U22	2IL14
U23-U25	2716
U26	7805K


U10 MC14411
U11 74LS74
U12,U15 74LS00
U14,U16 74LS30
U17 MC14584
U18 MC6840
U19 MC6809
U20 MC6808
U21,U22 21L14
U23-U25 2716
U26 7805K
A13
A14
A15
D0
D1
D2
D3
D4
D5
D6
D7
U25
U9
U8
U18
U20
U19
XTL2
C26
C27
R27
R26
R25
J14
J8
R7
R18
R/W
VMA
R5
E
Q
J4
RESET
J6
HALT
IRQ
FIRQ
J5
BS
BA
MRDY
MRST
NMI
R4
R3
R1
R19
R17
J7
R6
R9
J12



ELEKTRA 6808/6809 CPU	
CPU8/9	REV A
17 JAN 82	
J&M ELECTRONICS	


PARTS LIST
C1-C25 0.047 mfd.
C26,C27 24 pf.
C28,C29 1.0 mfd.
C30 2.2 mfd.
D1 IN4148
R1-R4,R6-R9 5.6K
R16,R17,R19,R24-R27 5.6K
R5,R11-R15 3.3K
R10 10M
R18 12K
R20,R21 100
R22,R23 390K
U1,U13 74LS04
U2,U4,U6 74LS244
U3,U8,U9 74LS240
U5 74LS260
U7 74LS138
U10 MC14411
U11 74LS74
U12,U15 74LS00
U14,U16 74LS30
U17 MC14584
U18 MC6840
U19 MC6809
U20 MC6808
U21,U22 2114
U23-U25 2716
U26 7805K
ELEKTRA 6808/6809 CPU
CPU8/9
REV A
17 JAN 82
J&M ELECTRONICS


PARTS LIST
C1-C25 0.047 mfd.
C26,C27 24 pf.
C28,C29 1.0 mfd.
C30 2.2 mfd.
D1 IN4148
R1-R4,R6-R9 5.6K
R16,R17,R19,R24-R27 5.6K
R5,R11-R15 3.3K
R10 10M
R18 12K
R20,R21 100
R22,R23 390K
U1,U13 74LS04
U2,U4,U6 74LS244
U3,U8,U9 74LS240
U5 74LS260
U7 74LS138
U10 MC14411
U11 74LS74
U12,U15 74LS00
U14,U16 74LS30
U17 MC14584
U18 MC6840
U19 MC6809
U20 MC6808
U21,U22 21L14
U23-U25 2716
U26 7805K
ELEKTRA 6808/6809 CPU
CPU8/9
REV A
17 JAN 82
J&M ELECTRONICS